Exhibit J

MacInnis 7,512,752 Applied to Representative Panasonic and Toyota Accused Products

This claim chart compares independent claim 1 of U.S. Patent No. 7,512,752 ("the MacInnis '752 patent") to Texas Instruments' DRA750 system on a chip ("SoC").

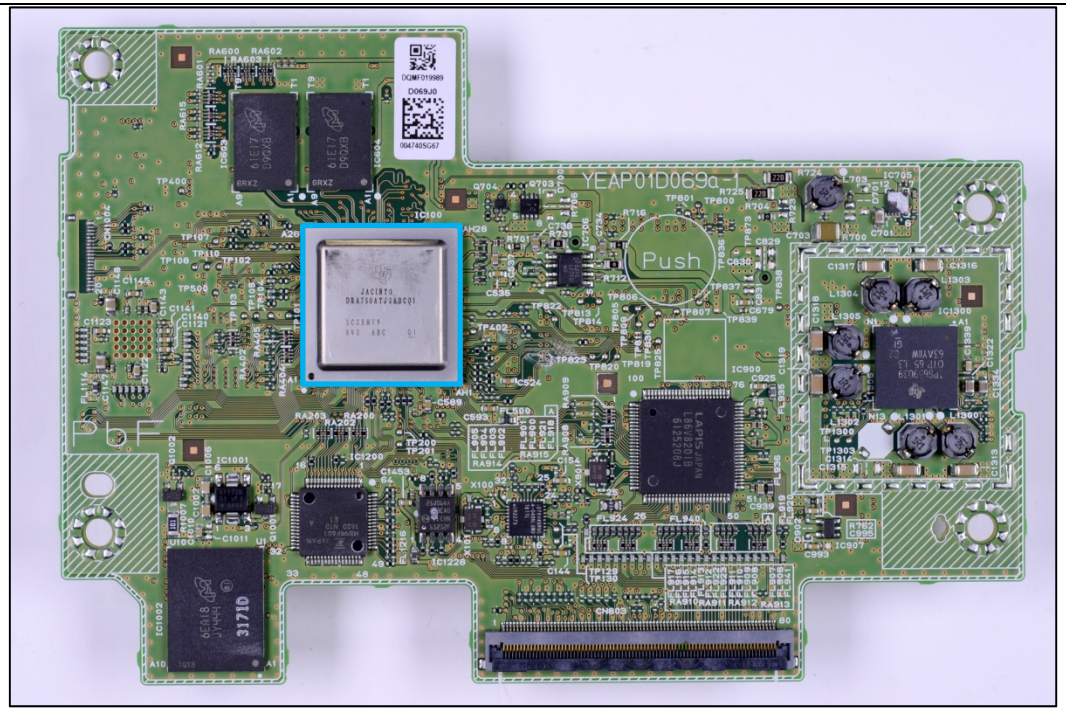
On information and belief, Texas Instruments' DRA750 SoC is representative of other Texas Instruments infotainment and high-end car information system SoCs having similar functionality ("Accused Texas Instrument Infotainment SoCs").

The DRA750 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser. Nos. 130105, 104020, 104069, 500021, which are incorporated in Accused Toyota Navigation units, including Highlander Receiver (86804-0E280), Sienna Navigation Unit (86804-08040), Avalon Navigation Head Unit (86804-07120), and Prius III Navigation System Kit (86804-47330), respectively.

On information and belief the Accused Texas Instrument Infotainment SoCs, and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs infringe directly, indirectly, and or under the doctrine of equivalents, at least claim 1 of the MacInnis '752 patent.

Claim - U.S. Patent No. 7,512,752 (MacInnis)	**Application of Claim Language to Accused Products**
Claim 1	
A memory access unit for accessing data for a module, said memory access unit comprising:	To the extent that the preamble is deemed limiting, the TI DRA750 SoC and downstream products include a memory access unit for accessing data for a module. At least the Panasonic (AT1501) head unit, which is included in at least the Toyota Prius III Navigation System Kit (225202), includes a Texas Instruments DRA750 SoC (highlighted in blue).


Model No. 86804-47330
Ref.No. CQ-XS05E0BJ
Set No. AT1501
DC 12V
Negative Ground
Speaker 4 Ω
Panasonic Corporation
Made in Japan
Serial No. 500021
CLASS 1
LASER PRODUCT
MANUFACTURED
JULY 2016



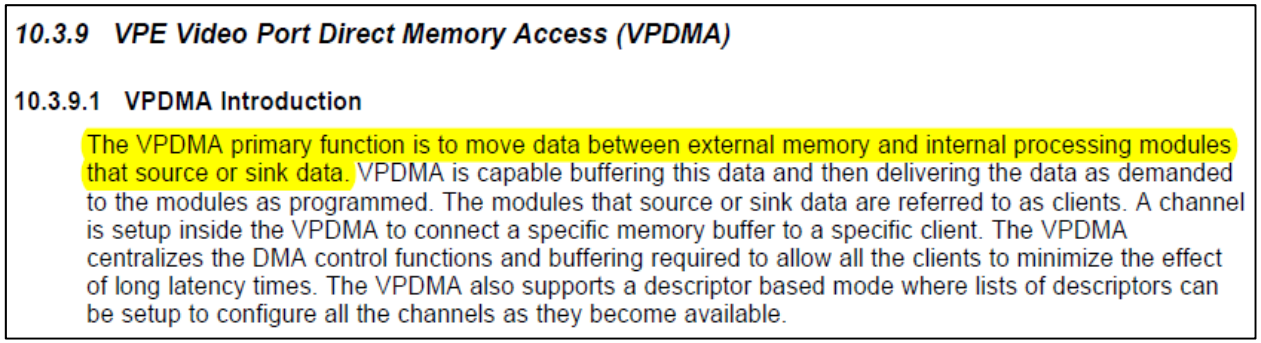
The TI DRA750 SoC includes a Video Port Direct Memory Access (VPDMA), which is a memory access unit for accessing data for a module. The VPDMA is included in the DRA750's Video Input Port (VIP) module and in the video processing engine (VPE).

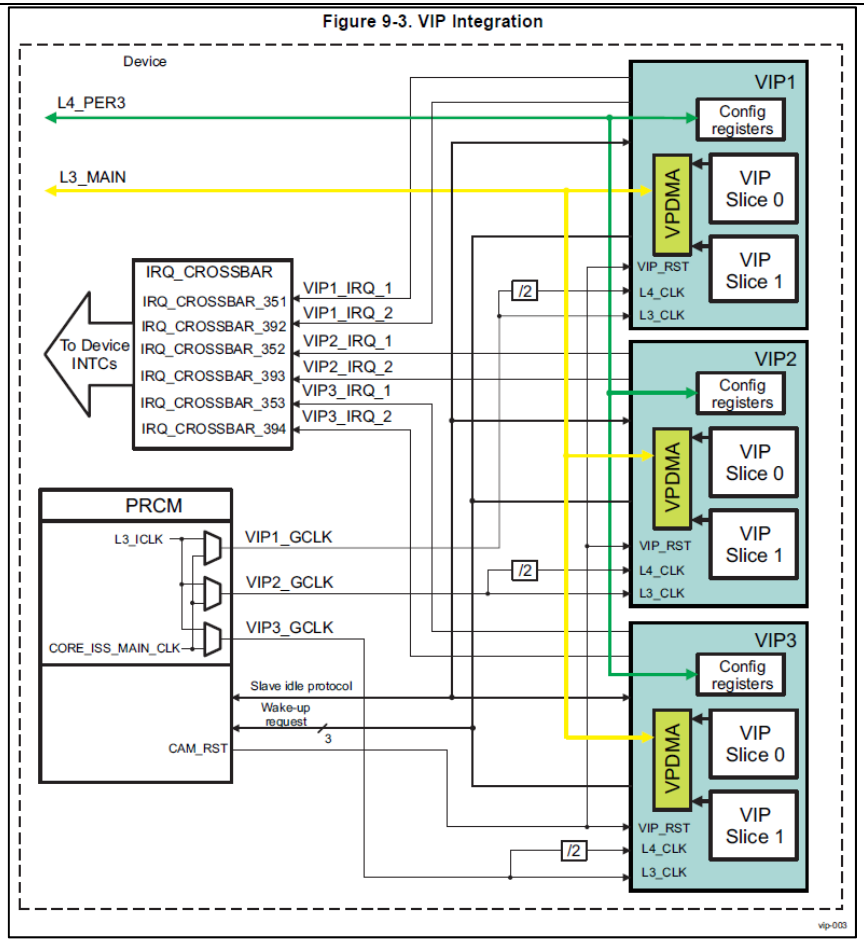
9.4.8 VIP Video Port Direct Memory Access (VPDMA)

9.4.8.1 VPDMA Introduction

The VPDMA primary function is to move data between external memory and internal processing modules that source or sink data. VPDMA is capable buffering this data and then delivering the data as demanded to the modules as programmed. The modules that source or sink data are referred to as clients. A channel is setup inside the VPDMA to connect a specific memory buffer to a specific client. The VPDMA centralizes the DMA control functions and buffering required to allow all the clients to minimize the effect of long latency times. The VPDMA also supports a descriptor based mode where lists of descriptors can be setup to configure all the channels as they become available.

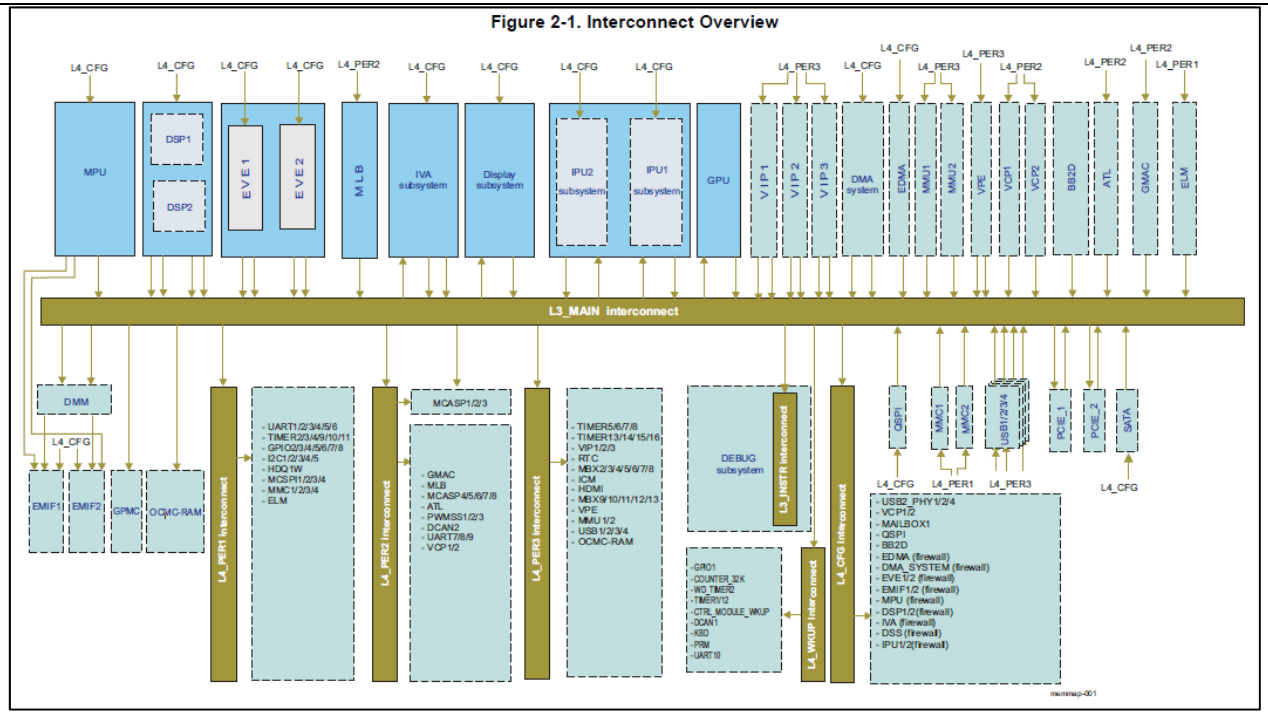
Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2198.

	 ***10.3.9 VPE Video Port Direct Memory Access (VPDMA)*** **10.3.9.1 VPDMA Introduction** The VPDMA primary function is to move data between external memory and internal processing modules that source or sink data. VPDMA is capable buffering this data and then delivering the data as demanded to the modules as programmed. The modules that source or sink data are referred to as clients. A channel is setup inside the VPDMA to connect a specific memory buffer to a specific client. The VPDMA centralizes the DMA control functions and buffering required to allow all the clients to minimize the effect of long latency times. The VPDMA also supports a descriptor based mode where lists of descriptors can be setup to configure all the channels as they become available. Exhibit 65 - DRA75x, DRA74x Technical Reference Manual at 2585.
an output port for providing access requests for lists of addresses in a memory over a link to a memory controller; and	The DRA750's Video Port Direct Memory Access (VPDMA) includes an output port for providing access requests for lists of addresses in a memory over a link to a memory controller. The VPDMA includes output ports for providing access requests for lists of addresses in a memory over the "L3_MAIN" link.



Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2104.

The VPDMA provides access requests for lists of addresses to memory controllers such as the “on-chip memory controller (OCMC)” and “general-purpose memory controller (GPMC).”



Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 383.

The VPDMA's output port provides for access requests for lists of addresses.

9.4.8.2.3 List

A list is a group of descriptors that makes up a set of DMA transfers that need to be completed. The VPDMA supports one kind of list only:

- The **Regular List** is a single list that the VPDMA will execute each descriptor once and initiate an interrupt when the list has completed. A regular list can contain any kind of descriptor without limitation and be of any size.

The VPDMA Controller works on lists of descriptors. In this mode the processor writes the lists of descriptors in the order it wants them executed. It then writes the location of the list to the VIP_LIST_ADDR register, followed by writing the size (bit LIST_SIZE) and type (bit LIST_TYPE) of the list, and list number (bit LIST_NUM) to the VIP_LIST_ATTR register. The List Manager module then schedules a DMA transfer to pull in the portion of the list that it can store in internal VPDMA memory. The List Manager will sequentially process the active list of descriptors until either the descriptor requires the use of a client that is currently active, or if it is waiting for the next portion of the list to be transferred from a DMA request. If there is no active list to process the list manager will go into an IDLE mode waiting for any client that is blocking a list or a list DMA transfer to complete.

All the DMA transfers are controlled by List Manager module inside VPDMA. List Manager needs to be loaded with FIRMWARE, before any DMA transfer from memory, after the VPDMA reset. The first MMR write to VIP_LIST_ADDR register after VPDMA reset should be the address of the memory buffer(128-bit aligned, that is, last four bits of the buffer address should be zero) where the firmware is stored. List Manager then schedules a DMA transaction to fetch the firmware and sets the VIP_LIST_ATTR[19] RDY bit after the firmware loading is complete.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2199 (highlighted).

9.4.8.7 VPDMA Descriptors

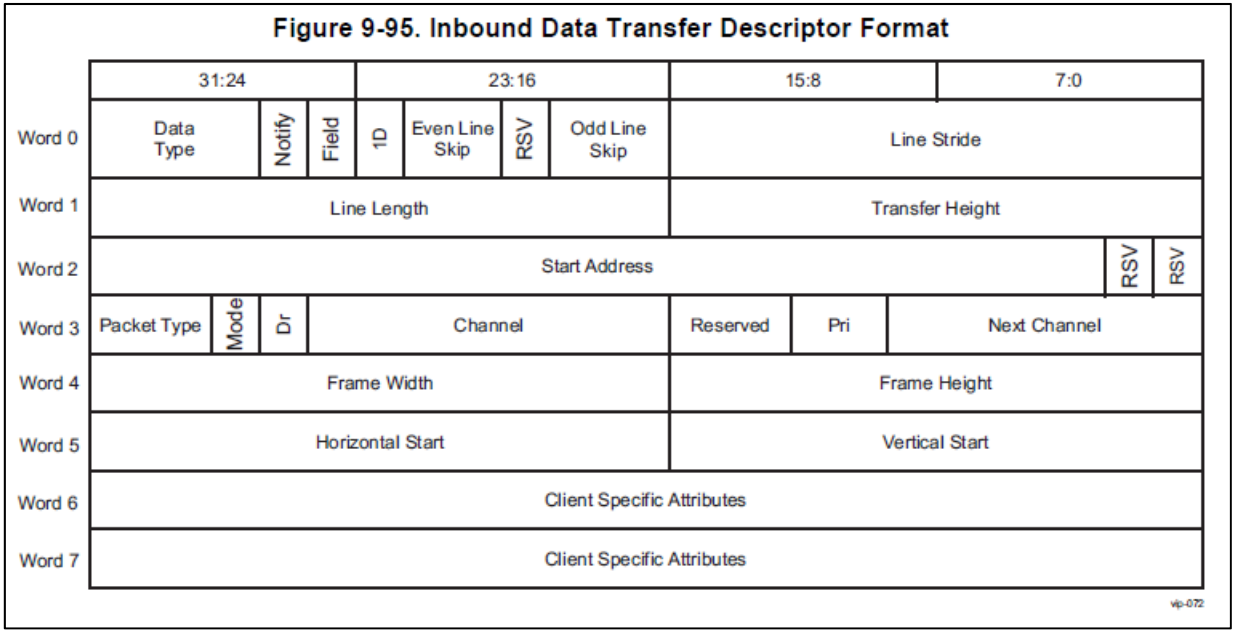
The VPDMA needs to be programmed through descriptors (a pre-defined structure of eight or four 32-bit words depending on type of descriptors) other than VPDMA Memory Mapped Registers (MMR). Descriptors are of three types:

i. **Data Transfer Descriptors** - A memory structure used to describe a desired memory transaction to or from a client.

ii. **Control Descriptors** - A memory structure used to perform a control operation inside the DMA controller

iii. **Configuration Descriptors** - A memory structure used to described a setup that should be applied to an processing modules like MMR write, scalar coefficient write etc.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2222 (highlighted).

	9.4.8.7.1 Data Transfer Descriptors In order to set up data transfers from the VPDMA, a data transfer descriptor is added into a list. The fields used for an Inbound and Outbound descriptor vary slightly. An outbound transfer can have two different outbound transfers. The two transfers are the main data transfer and a write of an Inbound Descriptor. The created inbound descriptor is formatted so it can be read back in directly to the next channel specified in the original descriptor. Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2223.  **Figure 9-95. Inbound Data Transfer Descriptor Format** 31:24 / 23:16 / 15:8 / 7:0 Word 0: Data Type; Notify; Field; 1D; Even Line Skip; RSV; Odd Line Skip; Line Stride Word 1: Line Length; Transfer Height Word 2: Start Address; RSV; RSV Word 3: Packet Type; Mode; Dr; Channel; Reserved; Pri; Next Channel Word 4: Frame Width; Frame Height Word 5: Horizontal Start; Vertical Start Word 6: Client Specific Attributes Word 7: Client Specific Attributes vip-072 Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2223.
a queue for queuing the access requests for the lists of addresses.	The DRA750's Video Port Direct Memory Access (VPDMA) includes a queue for queuing the access requests for the lists of addresses. For example, the VPDMA controller keeps the lists of descriptors in a queue until executed by the List Manager.

9.4.8.2.3 List

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The VPDMA Controller works on lists of descriptors. In this mode the processor writes the lists of descriptors in the order it wants them executed. It then writes the location of the list to the VIP_LIST_ADDR register, followed by writing the size (bit LIST_SIZE) and type (bit LIST_TYPE) of the list, and list number (bit LIST_NUM) to the VIP_LIST_ATTR register. The List Manager module then schedules a DMA transfer to pull in the portion of the list that it can store in internal VPDMA memory. The List Manager will sequentially process the active list of descriptors until either the descriptor requires the use of a client that is currently active, or if it is waiting for the next portion of the list to be transferred from a DMA request. If there is no active list to process the list manager will go into an IDLE mode waiting for any client that is blocking a list or a list DMA transfer to complete.

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Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2199 (highlighted).